CLAIM LISTING

Claims 1 – 24 (Canceled)

25. (Original) An analog-to-digital converter (ADC) comprising:

a source of an input voltage;

a source of a reference voltage;

a primary delay line connected to said source of an input voltage, and having a delay signal input and a plurality of tap outputs;

a timer delay line connected to said source of a reference voltage and having a timer signal input and a timer signal output;

a delay signal source connected to said delay signal input and said timer delay signal input, and

a digital output circuit coupled to said tap outputs and said timer signal output to provide a digital output indicative of a difference between said input voltage and said reference voltage.

26. (Original) The ADC of claim 25 wherein said ADC is implemented entirely with digital logic gates.

27. (Original) The ADC of claim 25 wherein said ADC includes no analog components.

28. (Original) The ADC of claim 25 wherein said primary delay line and said timer delay line are incorporated into a single integrated circuit.

29. (Original) The ADC of claim 25 wherein said primary delay line comprises a plurality of delay cells.

30. (Original) The ADC of claim 29 wherein each of said delay cells comprises a digital logic element.

31. (Original) The ADC of claim 25 wherein said timer delay line is substantially one-half the length of said primary delay line.

32. (Original) The ADC of claim 25 wherein said delay signal source simultaneously provides a delay signal to said delay signal input and a timer signal to said timer signal input.

33. (Original) The ADC of claim 32 wherein said delay signal and said timer signal as provided by said delay signal source are the same signal.

34. (Original) The ADC of claim 25 wherein said digital output circuit comprises an array of flip-flop circuits.

35. (Original) The ADC of claim 25 wherein said digital output circuit includes a counter.

36. (Original) The ADC of claim 25 wherein said digital output circuit includes a shift register.

37. (Original) The ADC of claim 25 wherein said primary delay line is a flat delay line.

38. (Original) The ADC of claim 25 wherein said primary delay line is a folded delay line.

39. (Original) The ADC of claim 25 wherein said primary delay line comprises a number of delay cells corresponding to the desired least significant bit (LSB) voltage step-size.

40. (Original) The ADC of claim 25 wherein said primary delay line comprises a number of delay cells smaller than the number of cells required to produce the desired least significant bit (LSB) voltage step-size.

41. (Original) The ADC of claim 25 wherein said timer delay line is a flat delay line.

42. (Original) The ADC of claim 25 wherein said timer delay line is a folded delay line.

43. (Original) The ADC of claim 25 wherein said digital output circuit includes a gain calibration circuit.

44. (Original) The ADC of claim 25 wherein said digital output circuit includes a mismatch correction circuit.

Claims 45 – 51 (Canceled)